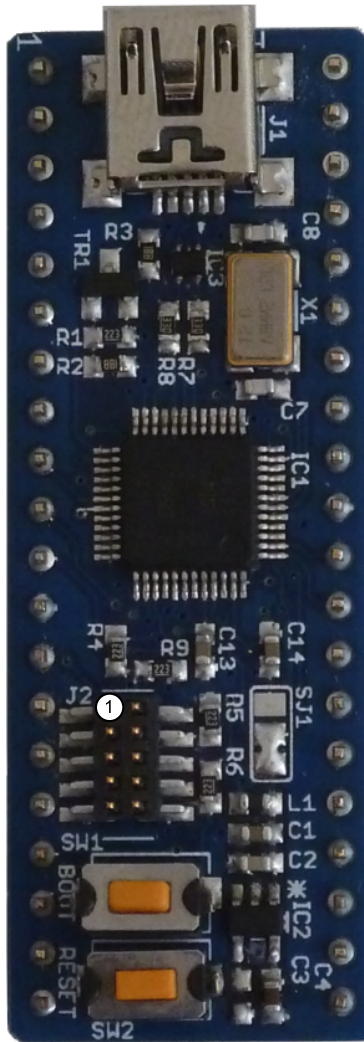


# DipCortex

P0_0 / Reset	1	⊗
P0_11 / AD0	2	⊗
P0_12 / AD1	3	⊗
P0_13 / AD2	4	⊗
P0_14 / AD3	5	⊗
P1_31	6	⊗
N/C	7	⊗
P0_16 / AD5	8	⊗
P0_22 / AD6	9	⊗
P0_23 / AD7	10	⊗
5V / 3.3V	11	⊗
GND	12	⊗
P1_29 / SCK0	13	⊗
P1_21 / MISO1	14	⊗
P0_8 / MISO0	15	⊗
P0_9 / MOSI0	16	⊗
P1_24 /	17	⊗
P0_4 / I2C SCL	18	⊗
P1_13	19	⊗
P1_14	20	⊗



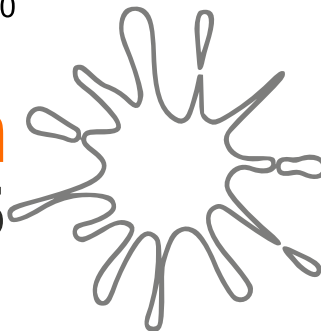
Q 40	P1_28
Q 39	P0_7
Q 38	P1_23 / SSEL1
Q 37	P1_20 / SCK1
Q 36	P1_27
Q 35	P1_26
Q 34	P0_2 / SSEL0
Q 33	P0_20
Q 32	5V/3.3V
Q 31	GND
Q 30	P1_19
Q 29	P1_25
Q 28	P1_16
Q 27	P1_15 / SCK1
Q 26	P0_18 / RX
Q 25	P0_19 / TX
Q 24	P0_21 / MOSI1
Q 23	P0_5 / I2C SDA
Q 22	P0_17
Q 21	P1_22

Pin No

Pin No

Boot button : PIO0\_1  
Reset button : PIO0\_0

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Notes : Pins have many other functions, please see datasheet  
Output voltage selectable via SJ1, 5v Pre Regulator or 3.3v Post Regulator  
Most General Purpose Inputs are 5V Tolerant, outputs when high are 3.3v  
Uses 10way Cortex Jtag header - SWD only  
Refer to NXP's processor datasheet for details